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10EC63

Sixth Semester B.E. Degree Examination, June/July 2014
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With a neat diagram, derive the expression for i_D in saturation and triode region. What happened to i_D if the channel length modulation is considered? **(10 Marks)**

b. Draw the large signal equivalent circuit model of NMOS and explain. **(04 Marks)**

c. Determine the voltages at all nodes and the currents through all the branches of following circuit. Let V_t = 1V and $kn'(W/L)$ = 1mA/V^2. Neglect the channel – length modulation effect. **(06 Marks)**

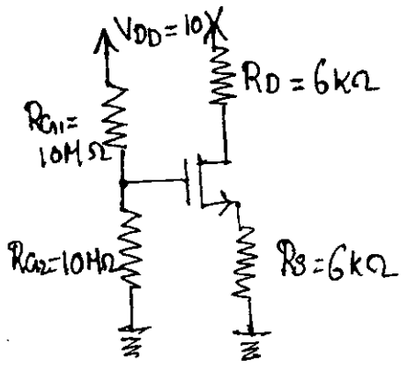

Fig.Q.1(c)

2 a. Show the development of the T equivalent – circuit model for the MOSFET from hybrid π model without channel length modulation. **(06 Marks)**

b. Draw the circuit of common-source amplifier with a source resistance. Draw its small signal equivalent circuit with γ_0 neglected. Obtain the expression for V_{gs}, id, v_o, A_v, A_{vo} and the overall voltage gain G_v. **(10 Marks)**

c. What is scaling? Differentiate constant field scaling and constant-voltage scaling. **(04 Marks)**

3 a. Briefly explain about short channel effect due to scaling. **(06 Marks)**

b. Compare NMOSFET and BJT in terms of
i) Current voltage characteristic.
ii) High frequency model.
iii) Output resistance. **(06 Marks)**

c. Following figure shoes the high frequency equivalent circuit of a common-source MOSFET amplifier. The amplifier is fed with a signal generator Vsig having a resistance Rsig. Resistance R in is due to the biasing network. Resistance R'_L is the parallel equivalent of the load resistance RL, the drain bias resistance R_D, and the FET output resistance ro. Capacitors cgs and cgd are the MOSFET internal capacitance:

i) Draw the equivalent circuit at midband frequencies.
ii) Draw the circuit for determining the resistance seen by Cgs.
iii) Draw the circuit for determining the resistance seen by Cgd. For Rsig = 100KΩ, Rin = 420KΩ, Cgs = Cgd = 1pF, gm = 4mA/V, and R'_L = 3.33KΩ
iv) Find the mid band voltage gain $A_M = V_0/Vsig$.
v) Find the upper 3-dB frequency f_H. **(08 Marks)**

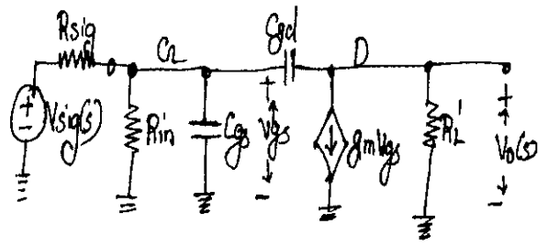

Fig.Q.3(c)

4 a. In common-gate amplifier with active load, obtain 3-dB frequency f_H using open circuit time constants. Draw the circuit required for determining Rgs and Rgd. **(08 Marks)**
b. Draw the $C_D - C_S$, $C_D - C_E$ and $C_D - C_a$ configurations. **(06 Marks)**
c. Draw an I_C source follower circuit. Obtain its small signal equivalent circuit and obtain its voltage gain $A_V = \frac{V_0}{V_i}$. **(06 Marks)**

PART – B

5 a. Obtain common-gate and common-mode rejection ratio (CMRR) of the MOS differential amplifier. Also find the effect of R_D mismatch on CMRR. **(12 Marks)**
b. Draw the two-stage CMOS op-amp configuration and briefly explain. Obtain overall dc open-loop gain. **(08 Marks)**

6 a. Briefly explain about
i) Voltage amplifier
ii) Current amplifier
iii) Trans conductance amplifier
iv) Trans resistance amplifier. **(08 Marks)**
b. Explain about series-shunt feedback amplifier with diagram and obtain the expression for input impedance and output impedance. **(08 Marks)**
c. Briefly explain about stability and pole locations. **(04 Marks)**

7 a. Draw and explain about weighted summer capable of implementing summing coefficients of both signs. **(06 Marks)**
b. Explain about DC imperfections. **(04 Marks)**
c. Write short notes on:
i) Antilogarithmic amplifiers.
ii) Analog multipliers. **(10 Marks)**

8 a. Draw the CMOS realization of A01 gate and explain with truth table. **(08 Marks)**
b. Draw and explain the exclusive OR function using PUN and PDN. **(08 Marks)**
c. What all are the parameters used to characterize the operation and performance of a logic circuit family. **(04 Marks)**

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